

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of:
Christopher Alan Menkus

Patent No.: 7,088,281

Issued: August 8, 2006

For: COARSE CHANNEL CALIBRATION FOR
FOLDING ADC ARCHITECTURES

**REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 CFR 1.323 AND 1.322**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Upon reviewing the above-identified patent, Patentee noted typographical errors which should be corrected. A listing of the errors to be corrected is attached.

The typographical errors marked with a "P" on the attached list are not in the application as filed by applicant. Also given on the attached list are the documents from the file history of the subject patent where the correct data can be found.


The errors now sought to be corrected are inadvertent typographical errors the correction of which does not involve new matter or require reexamination.

Transmitted herewith is a proposed Certificate of Correction effecting such corrections. Patentee respectfully solicits the granting of the requested Certificate of Correction.

The Commissioner is authorized to charge any deficiency of up to \$300.00 or credit any excess in this fee to Deposit Account No. 04-0100.

Dated: February 20, 2007

Respectfully submitted,

By 
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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. : 7,088,281
APPLICATION NO. : 10/757,750
ISSUE DATE : August 8, 2006
INVENTOR(S) : Christopher Alan Menkus

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

First Page Col. 2 (U.S. Patent Documents); Line 8; After "6,628,216" delete "B1" and insert -- B2 --, therefor.

Column 4; Line 19; Delete "bcout1" and insert -- bcoutl --, therefor.

Column 4; Line 28 (Approx.); Delete "ADJ 1-ADJK." and insert -- ADJ1-ADJK. --, therefor.

Column 4; Line 29 (Approx.); Delete "ADJ 1-ADJK" and insert -- ADJ1-ADJK --, therefor.

Column 6; Line 26; Delete "bcout1" and insert -- bcoutl --, therefor.

Column 6; Line 27; Delete "bcout1." and insert -- bcoutl. --, therefor.

Column 6; Line 38; After "signal" delete "cout1." and insert -- coutl. --, therefor.

Column 6; Line 38; Before "has" delete "cout1" and insert -- coutl --, therefor.

Column 6; Line 46; Delete "cout1" and insert -- coutl --, therefor.

Column 6; Line 51; Delete "bcout1" and insert -- bcoutl --, therefor.

Column 6; Line 52; Delete "cout1." and insert -- coutl. --, therefor.

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Column 7; Line 5; Delete "bcout1" and insert - - bcoutl - -, therefor.

Column 7; Line 6; Delete "bcout1" and insert - - bcoutl - -, therefor.

Column 7; Line 10; Delete "bcout1" and insert - - bcoutl - -, therefor.

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Issued Patent Proofing Form		File#: 08211/0200349-US0	
Note: P = PTO Error		A = Applicant Error	
US Serial No.: 10/757,750		US Patent No.: US 7,088,281 B1	
Title: COARSE CHANNEL CALIBRATION FOR FOLDING ADC ARCHITECTURES		Issue Dt.: Aug. 8, 2006	

Sr. No.	P/A	Original		Issued Patent		Description Of Error
		Page	Line	Column	Line	
1	P	Page 1 of 1 List of references cited by examiner (08/15/2005)	Entry 1 (U.S. Patent Documents)	First Page Col. 2 (U.S. Patent Documents)	8	After "6,628,216" delete "B1" and insert - - B2 - -, therefor.
2	P	Page 6 Specification (01/14/2004)	3	4	19	Delete "bcout1" and insert - - bcoutl - -, therefor.
3	P	Page 6 Specification (01/14/2004)	10	4	28 (Approx.)	Delete "ADJ 1-ADJK." and insert - - ADJ1-ADJK. - -, therefor.
4	P	Page 6 Specification (01/14/2004)	10	4	29 (Approx.)	Delete "ADJ 1-ADJK" and insert - - ADJ1-ADJK - -, therefor.
5	P	Page 9 Specification (01/14/2004)	8	6	23	Delete "bcout1" and insert - - bcoutl - -, therefor.
6	P	Page 9 Specification (01/14/2004)	11	6	27	Delete "bcout1." and insert - - bcoutl. - -, therefor.
7	P	Page 9 Specification (01/14/2004)	18	6	38	After "signal" delete "cout1." and insert - - coutl. - -, therefor.
8	P	Page 9 Specification (01/14/2004)	18	6	38	Before "has" delete "cout1" and insert - - coutl - -, therefor.
9	P	Page 9 Specification (01/14/2004)	23	6	46	Delete "cout1" and insert - - coutl - -, therefor.
10	P	Page 9 Specification (01/14/2004)	27	6	51	Delete "bcout1" and insert - - bcoutl - -, therefor.
11	P	Page 9 Specification (01/14/2004)	27	6	52	Delete "cout1." and insert - - coutl. - -, therefor.
12	P	Page 10 Specification (01/14/2004)	10	7	5	Delete "bcout1" and insert - - bcoutl - -, therefor.
13	P	Page 10 Specification (01/14/2004)	11	7	6	Delete "bcout1" and insert - - bcoutl - -, therefor.

14	P	Page 10 Specification (01/14/2004)	14	7	10	Delete "bcout1" and insert - - bcout1 - -, therefor.
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(12) United States Patent
Menkus**(10) Patent No.: US 7,088,281 B1**
(45) Date of Patent: Aug. 8, 2006

- (54) **COARSE CHANNEL CALIBRATION FOR FOLDING ADC ARCHITECTURES**
- (75) Inventor: Christopher Alan Menkus, Munich (DE)
- (73) Assignee: National Semiconductor Corporation, Santa Clara, CA (US)
- (*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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H03M 1/12 (2006.01)

(52) U.S. Cl. 341/156; 341/120; 341/118

(58) Field of Classification Search 341/155, 341/156, 159, 161, 120, 118; 314/118, 120
See application file for complete search history.(56) **References Cited****U.S. PATENT DOCUMENTS**

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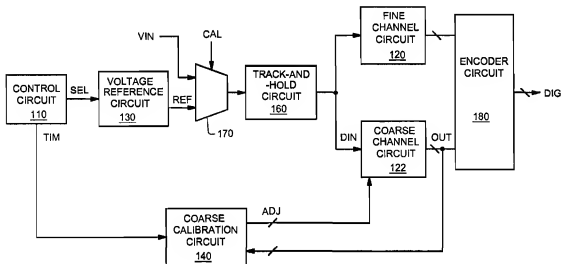
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(57) **ABSTRACT**

A circuit for calibrating a coarse channel circuit in a folding analog-to-digital converter circuit. A reference value is input to the coarse channel circuit and an output of the coarse channel circuit is sensed. A parameter of the coarse channel circuit is adjusted until the coarse channel circuit is successfully calibrated.

22 Claims, 8 Drawing Sheets100

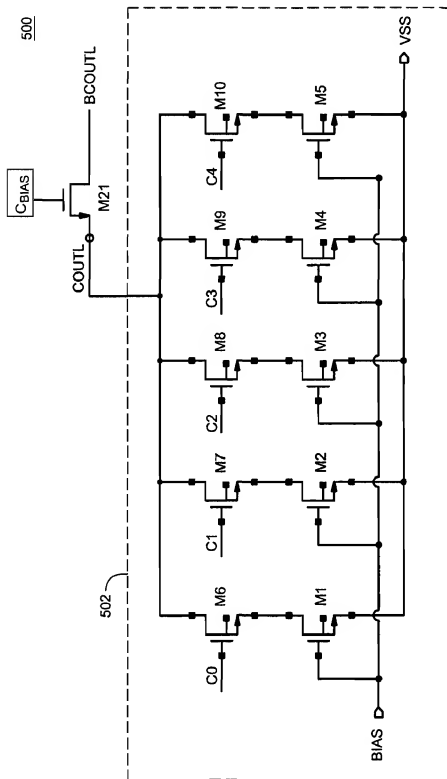


Figure 5B

of encoder circuit 180. Encoder circuit 180 is configured to provide signal DIG using signal information from both coarse channel circuit 122 and fine channel circuit 120. In one embodiment, coarse channel circuit 122 is a (non-folded) flash ADC. Also, fine channel circuit 120 includes folding stages. Additionally, since encoder circuit 180 is not employed during the calibration process, it may be disabled if signal CAL corresponds to the second logic level, such that signal DIG is not provided.

Control circuit 110 is configured to provide a select signal (SEL) for selecting a voltage reference. Further, control circuit 110 is arranged to assert a timing signal (TIM) for latching coarse channel calibration circuit 140 at a pre-determined amount of time after it changes the select signal (SEL). For example, signal TIM may be asserted after a pre-determined settling time has occurred.

Voltage reference circuit 130 is configured to provide signal REF, which is associated with signal SEL. In one embodiment, voltage reference circuit 130 includes a relatively accurate voltage reference subdivided across a resistor ladder, and CMOS switches to select one of the reference voltages. In other embodiments, reference circuit 130 may have different architectures.

Track-and-hold circuit 160 is configured to receive signal REF during calibration. Coarse channel circuit 122 is configured to receive an output signal from track-and-hold circuit 122. Coarse channel circuit 122 is further configured to provide an output signal (OUT) in response to the output signal from the track-and-hold circuit. Signal OUT includes a plurality of comparator outputs (COMPOUT1-COMPOUTK) (as shown in more detail in FIG. 2). K is the number of comparators in coarse channel circuit 122. Any desired number of reference voltages may be tested during the calibration. According to one embodiment, one reference voltage is tested during calibration. However, in another embodiment, a reference voltage associated with each code transition of signal DIG is tested for calibration. According to yet another embodiment, a reference voltage associated with each folded region transition is tested for calibration. In one embodiment, coarse channel circuit 122 is arranged to process the DIN signal at substantially the same conversion speed that is used during encoding.

Also, in one embodiment, coarse channel circuit 122 is arranged to provide a feedback signal (FB). According to one embodiment, the FB signal includes at least a portion of the OUT signal. In another embodiment, although not shown, signal FB may be provided by an off-chip digital signal processor (DSP).

Further, coarse channel calibration circuit 140 is arranged to receive the FB signal. Coarse channel calibration circuit 140 is further arranged to latch the FB signal in response to the assertion of the TIM signal. Coarse channel calibration circuit 140 is further arranged to provide an adjustment signal (ADJ) to coarse channel calibration circuit 140 in response to the FB signal. Additionally, coarse channel calibration circuit 140 is configured to adjust a parameter of coarse channel circuit 122 via the ADJ signal, until the OUT signal is successfully calibrated for the currently selected voltage reference signal (REF).

FIG. 2 shows a block diagram of an exemplary embodiment of coarse channel circuit 122 as illustrated in FIG. 1. In this embodiment, coarse channel circuit 122 is shown to include a coarse reference circuit (210), an amplifier array (220), and a comparator array (230). Coarse reference circuit 210 may include a resistor ladder, other means of generating reference voltages, and the like. Amplifier array 220

includes an array of K amplifiers, including amplifier 221. Comparator array 230 includes an array of K comparators. Coarse reference circuit 210 is configured to provide a plurality of coarse reference voltages. The plurality of coarse voltage references are spaced corresponding to the voltage spacing between each folded region of the fine channel circuit. Comparator array 230 is configured to compare signal DIN with each of the plurality of coarse reference voltages, if amplifier array 220 is not included in coarse channel circuit 122. If amplifier array 220 is included in coarse channel circuit 122, amplifier array 220 is configured to increase the signal amplitude before the comparison is made such that smaller comparators may be used in comparator array 230. Although only one amplifier array is shown in FIG. 2, in another embodiment coarse channel circuit 122 may contain no amplifier arrays, one or more additional amplifier arrays, and the like.

Amplifier array 220 is configured to receive signal ADJ (e.g. signals bcout1 and bcout, as described below). However, in another embodiment, signal ADJ may be received by another part of coarse channel circuit 122, such as a subsequent amplifier stage (not shown), comparator array 230, and the like.

According to another exemplary embodiment, signal ADJ includes K differential signals, ADJ1-ADJK. In this case, amplifier array 220 would include K amplifiers where each of the K amplifiers is configured to receive a corresponding one of the differential signals ADJ1-ADJK. Also, each of the differential signals ADJ1-ADJK may comprise a differential current, where each differential current is provided by a corresponding pair of current DACs. According to other embodiments, signal ADJ can include virtually any number of differential signals, or only one differential signal. According to one embodiment, signal ADJ includes one or more differential signals. According to another embodiment, signal ADJ includes one or more single-ended signals.

FIG. 3A illustrates a block diagram of an exemplary embodiment of coarse channel adjustment circuit 140. In this embodiment, coarse channel adjustment circuit 140 includes seven calibration circuits (e.g. 341-347). In another embodiment (not shown), coarse channel adjustment circuit may include only one calibration circuit (341). In yet another embodiment, coarse channel adjustment circuit 140 may include a plurality of calibration circuits substantially equivalent to the number (K) of comparators in the coarse channel circuit. In still another embodiment, coarse channel adjustment circuit 140 may include some other number of calibration circuits. In any case, coarse channel adjustment circuit 140 is configured to receive the FB signal. Also, in one embodiment, the OUT signal is arranged to also be the FB signal for coarse channel adjustment circuit 140.

FIG. 3B shows a block diagram of an exemplary embodiment of calibration circuit 341 which includes a counter circuit (302) and a parameter adjustment circuit (304). Counter circuit 302 is coupled to coarse channel circuit 122. Also, parameter adjustment circuit 304 is coupled to counter circuit 302 and coarse channel circuit 122.

Signal COUNT includes signal COUNT1, signal FB includes signal FB1, and signal ADJ includes signal ADJ1. Also, counter circuit 302 is configured to provide signal COUNT1 in response to signal FB1 and signal TIM. Parameter adjustment circuit 304 is configured to receive signal COUNT1 and adjust the parameter of coarse channel circuit 122 in response to signal COUNT1. Counter circuit 302 is configured to, if latched by signal TIM: increment a count value that is associated with signal COUNT1 if signal FB1

corresponds to a first logic level, and decrement the count value if signal FB1 corresponds to a second logic level.

According to one embodiment, signal COUNT includes signals (COUNT1-COUNTK), signal FB includes signals FB1-FBK, and signal ADJ includes signals ADJ1-ADJK. In this embodiment, coarse channel circuit 122 includes K counter circuits and K parameter adjustment circuits. Each of the K counter circuits provides a corresponding signal COUNT1-COUNTK in response to a corresponding comparator output signal COMPOUT1-COMPOUTK. Each of the K parameter adjustment circuits receives a corresponding signal COUNT1-COUNTK and provides a corresponding signal ADJ1-ADJK.

Counter circuit 302 is configured to be latched by signal TIM to allow timing requirements (e.g., settling time) to be met. Control circuit 110 is configured to provide signal TIM at a pre-determined period of time after signal SEL is changed such that the timing requirements are met.

According to one embodiment, counter circuit 302 is a bi-directional counter, and the like. However, in another embodiment, counter circuit 302 may be a uni-directional counter, and the like.

FIG. 4 illustrates a flow chart of an exemplary process of coarse channel calibration (400) for a folding ADC architecture.

After a start block, the process proceeds to block 402 where a voltage reference is selected. At block 404, the process waits for a settling period of time to finish. Next, the process steps to block 406 where a comparator output for the coarse channel circuit is latched. From block 406 the process advances to decision block 408, where a determination is made as to whether the comparator output corresponds to a first logic level. If no, the process moves to block 410 where the count value of the counter circuit is decremented (e.g., by one). Next, the process proceeds to block 412 where a parameter of the coarse channel circuit is decreased. From block 412, the process moves to a return block and returns to performing other actions.

However, if the determination at decision block 408 was affirmative (i.e., if the comparator output corresponds to a second logic level), the process would have moved to block 414 where the count value would be incremented (e.g., by one). Next, the process would advance to block 416 where the parameter of the coarse channel circuit would be increased. Next, the process would proceed to the return block and return to performing other actions.

The process may be repeated for each reference voltage. In one embodiment, a different reference voltage would be selected for each iteration of the process. In another embodiment, the process would be repeated several times for the same reference voltage. The number of iterations to ensure a full range of calibration would be dependent on the number of bits used by the counter circuit. A counter circuit with a larger number of bits would enable a greater resolution in the calibration, but require a greater number of iterations to ensure that the full calibration range is reached. Once calibration is successfully completed, the comparator output can toggle between a logical one and a logical zero. Accordingly, a successful calibration enables the OUT signal to have an error corresponding to one least significant bit of the count value. This error can be made small compared to the allowable tolerance by adjusting the smallest adjustment step size.

Prior to beginning process 400, the count value may be reset to a mid-point value. In this way, less iterations may be required to cover the full calibration range. For example, a five-bit bi-directional counter may be used, with the count

value being reset to a mid-point value (e.g., binary number 10000) before initiating process 400. A minimum of sixteen iterations would be required for the count value to go from 10000 to 00000. If the count value was not reset at the beginning of the calibration, a minimum of 31 iterations would be required to ensure covering the full calibration range. For example, the count value could initially be at 00000, and a minimum of 31 iterations would be required to go from 00000 to 11111.

Additionally, process 400 may be performed for one, some, or all of the comparators in the coarse channel circuit. Also, according to the embodiment illustrated in FIG. 4, the parameter is decreased if the count value is decremented, and increased if the count value is incremented. In yet another embodiment, the parameter may be increased if the count value is decremented, and decreased if the count value is incremented.

FIG. 5A shows an exemplary embodiment of parameter adjustment circuit 304. In this embodiment, parameter adjustment circuit 304 includes a first current DAC circuit (500), and a second current DAC circuit (550). In this exemplary embodiment, signal ADJ is a differential signal that includes signals bcount1 and bcount. In this embodiment, signal COUNT is a five-bit signal. Signal COUNT includes signals c0-c4. An inverted count signal includes signals c0b-c4b. DAC circuit 500 is further configured to convert signal COUNT into signal bcount1. Also, DAC circuit 550 is configured to convert the inverted count signal (c0b-c4b) into signal bcount. Additionally, DAC circuit 500 and DAC circuit 550 may include substantially equivalent architectures.

FIG. 5B schematically illustrates an exemplary embodiment of current DAC circuit 500. Current DAC circuit 500 includes a current DAC (502) and transistor M21. Transistor M21 is an optional circuit element for current DAC circuit 500. Also, current DAC 502 includes transistors M1-M10. Current DAC 502 is configured to convert signal COUNT into signal bcount1. Signal bcount1 has an associated analog current.

Transistors M6-M10 are each configured to operate as a switch. Transistors M6-M10 are each configured to be on when its gate terminal is at an active level, and off when its gate terminal is at an inactive level. Transistors M1-M5 are each configured to provide a scaled current. For example, transistors M1-M5 may each be scaled at a ratio of 32:16:8:4:1. Accordingly, the current associated with signal bcount1 is decoded according to signal COUNT, and the current associated with signal bcount is decoded according to the inverted count signal.

Optional transistor M21 is configured to operate as a cascode transistor and provide signal bcount1 in response to signal bcount1. Transistor M21 is configured to operate as a current buffer. Additionally, bias signal bcbias is a cascode bias signal for transistor M21.

FIG. 6 schematically illustrates an exemplary embodiment of amplifier 221. Amplifier 221 is configured to receive a differential coarse reference voltage (REFP, REFN) and a coarse channel input signal (DIN, which includes INN and INP). In one embodiment, the DIN signal is a differential signal. In another embodiment, the DIN signal is a single-ended signal. OTA 690 in amplifier 221 is further configured to provide a differential output current. To convert the differential current to a differential output voltage, a first load (R1) is configured to receive a first half of the differential output current, and a second load (R2) is configured to receive a second half of the differential output current. Although loads R1 and R2 are shown as resistors, other

types of loads may be used for loads R1 and R2, including, but not limited to, transistors.

In one embodiment, the parameter adjustment circuit (304) shown in FIG. 5A is coupled to amplifier 221 such that signal bcout1 is provided at load R1, and signal bcout1 is provided at load R2. In other embodiments, signals bcout1 and bcout1 may be coupled to amplifier 221 in a different manner. The differential output voltage is determined according to signals REFP, REFN, INN, and INP, and is further modified by signals bcout1 and bcout1 to adjust for offset error. The offset error may be caused by process variation, threshold variation, and the like. Offset error may result from any component, including track-and-hold circuit 160, coarse voltage reference ladder 210, amplifier array 220, other amplifier arrays, and comparator array 230. Amplifier and comparator offsets, as well as mismatch in resistor values and current mirror ratios, can all contribute to the total offset error. Although offset error can result from multiple components, the total offset error may be corrected at one point in the chain of components.

The above specification, examples and data provide a description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention also resides in the claims hereinafter appended.

What is claimed is:

1. A circuit for analog-to-digital conversion, comprising:
a fine channel circuit that includes folding stages;

a coarse channel circuit; and

a coarse channel calibration circuit that is coupled to the coarse channel circuit,

wherein the coarse channel calibration circuit includes:

a counter circuit that is coupled to the coarse channel circuit; and

a parameter adjustment circuit that is coupled to the counter circuit and the coarse channel circuit, wherein

the coarse channel circuit is configured to provide a feedback signal,

the counter circuit is configured to:

receive the feedback signal, and

provide a count signal in response to the feedback signal, and wherein

the parameter adjustment circuit is configured to:

receive the count signal, and

adjust a parameter of the coarse channel circuit in response to the count signal, and

wherein the counter circuit is configured to, if latched:

increment a count value that is associated with the count signal if the comparator output corresponds to a first logic level, and

decrement the count value if the comparator output corresponds to a second logic level.

2. The circuit of claim 1, further comprising:

a control circuit that is configured to provide a select signal; and

a voltage reference circuit that is configured to provide a voltage reference signal that corresponds to the select signal, wherein

the coarse channel circuit is configured to receive the voltage reference signal.

3. The circuit of claim 1,

wherein the coarse channel circuit is configured to provide an output signal in response to a voltage reference signal.

4. The circuit of claim 3,

wherein the output signal includes the feedback signal.

5. The circuit of claim 1,

wherein the coarse channel circuit comprises an amplifier array and a comparator array, and

wherein at least one of the amplifier array or the comparator array is configured to receive an adjustment signal.

6. The circuit of claim 5,

wherein the coarse channel calibration circuit is configured to:

provide the adjustment signal to the coarse channel circuit in response to the feedback signal.

7. The circuit of claim 1,

wherein the parameter adjustment circuit includes a digital-to-analog converter circuit, and

wherein the digital-to-analog converter circuit is configured to provide a converted signal to the coarse channel circuit.

8. The circuit of claim 1,

wherein the parameter comprises one of a single-ended current or differential current.

9. The circuit of claim 1, wherein

the fine channel circuit is arranged to perform a fine analog-to-digital conversion of an input signal; and wherein the coarse channel circuit is arranged to perform a coarse analog-to-digital conversion of the input signal in parallel with fine analog-to-digital conversion.

10. The circuit of claim 1, wherein

the coarse channel circuit is arranged to perform a coarse analog-to-digital conversion; and wherein the coarse channel calibration circuit is arranged to calibrate the coarse analog-to-digital conversion.

11. The circuit of claim 1,

wherein the coarse channel circuit includes an amplifier array.

12. A circuit for analog-to-digital conversion, comprising:

a fine channel circuit that includes folding stages;

a coarse channel circuit; and

a coarse channel calibration circuit that is coupled to the coarse channel circuit,

wherein the coarse channel calibration circuit includes:

a counter circuit that is coupled to the coarse channel circuit; and

a parameter adjustment circuit that is coupled to the counter circuit and the coarse channel circuit, wherein

the coarse channel circuit is configured to provide a feedback signal,

the counter circuit is configured to:

receive the feedback signal, and provide a count signal in response to the feedback signal, and wherein

the parameter adjustment circuit is configured to:

receive the count signal, and

adjust a parameter of the coarse channel circuit in response to the count signal, and

wherein the parameter adjustment circuit includes:

a first digital-to-analog converter circuit that is configured to convert the count signal into a first analog signal; and

a second digital-to-analog converter circuit that is configured to convert an inverted count signal into a second analog signal.

13. The circuit of claim 12, wherein

the coarse channel circuit includes an amplifier that is configured to provide a differential output current,